ABSTRACT

A comparison circuit that reduces the penetration current in the internal part of the comparison circuit is disclosed. The circuit also reduces the penetration current in the circuit that is connected to the next stage. The amplification circuit of the comparison circuit comprises an amplifier that outputs a digital signal after amplifying the input analog signal. The input analog signal that has a voltage that differs from the predetermined voltage in the 1st time period and the predetermined voltage in the 2nd time period. A first switch stops the supply of electric power to the amplifier in the 1st time period, and a second switch fixes the output of the said amplifier to the predetermined voltage in the 1st time period.